wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width, and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

Remarks

Applicants affirm the election of claims 1-12 (Group I) in response to a telephone conversation with the Examiner. Claims 13-21 (Group II) will be prosecuted in a divisional application.

Claims 2-6 and 8-12 are presently active, claims 1 and 7, and claims 13-21 (Group II), having been cancelled by this Amendment without prejudice.

Because of a restriction requirement, election was made not to prosecute claims 13-21 (Group II). Accordingly, it was necessary to delete Luiz M. Franca-Neto as an inventor because his invention is not being prosecuted in this application.

In the office action dated 11 April 2002 ("Office Action"), claims 1, 2, 4, 7, 8, and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by Sudo et al., U.S. patent 5,812,018 ("Sudo"); claims 3, 5, 6, 9, and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sudo; and claims 6 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art (Figs. 1-4 in the present application), in view of Nakano, U.S. patent 5,917,366 ("Nakano").

Applicants believe all presently active claims as amended by this amendment are patentable over the cited references. Each of the claim rejections are discussed below.

35 U.S.C. §102(b) rejection of claims 1, 2, 4, 7, 8, and 10 over Sudo

Claim 1 is cancelled without prejudice, and claim 2 is rewritten to include the limitations of claim 1. Claim 2 of the present invention recites the limitation that "the gate and the first terminal [of the FET] are each connected to the input port, and the second terminal is connected to the output port so that the output voltage is indicative of a local time-average maximum of the input signal voltage."

The claim rejection in the Office Action refers to Fig. 1 of Sudo. In Fig. 1, Sudo teaches how a negative high voltage VBB and a positive high voltage VPP may be generated from the power supply voltage VCC. (See Sudo, the Abstract and column 1, lines 37 - 67.) Nowhere does Sudo teach a circuit having an output voltage that is indicative of a local time-average maximum. The negative high voltage VBB is not a local time-average maximum of the positive high voltage VPP or the power supply voltage VCC, and the positive high voltage VPP is not a local time-average maximum of the negative high voltage VBB or the power supply voltage VCC.

Claim 2 may be further distinguished from Sudo. Claim 2 recites that the "second terminal [of the FET] is connected to the output port." However, in Fig. 1 of Sudo, the output port VPP is not connected to a terminal of transistor M11. Instead, there are several transistors connected between output port VPP and transistor M11 with gates clocked by clock signals.

Claim 2 may be further distinguished over Sudo. Claim 2 recites that in steady state, the FET operates in its sub-threshold region if the input signal voltage is stationary. When a transistor is operated in its sub-threshold region, there may be leakage current present when the transistor has zero gate-to-source voltage and the magnitude (absolute value) of the drain-to-source voltage is greater than zero. Leakage current becomes a problem when threshold voltages and device sizes become very small, such as, for example, in the neighborhood of 0.1 microns in device width. The present invention is believed to be novel because it takes advantage of leakage current to perform maximum or minimum detection. Because the FET operates in its sub-threshold region if the input signal voltage is stationary, the flow of leakage current allows the voltage on a capacitive load to track the local time-average maximum of the input signal voltage.

The circuit (Fig. 1) of Sudo is a voltage booster circuit, and it may be inferred that the transistors in this circuit do not operate in their sub-threshold region, for otherwise, there wouldn't be enough current provided at output ports VBB and VPP to drive circuits or loads connected to these output ports. One of ordinary skill in the art would infer that the devices taught in Sudo operate in their active regions. The circuit of Sudo is not relevant to the present invention. There simply is no motivation, upon reading Sudo, to

practice the claimed invention for which the FET operates in its sub-threshold region when in steady state and when the input signal voltage is stationary.

Accordingly, claim 2 is believed to be patentable over Sudo.

Claim 4 is also distinguishable over Sudo because it recites that the second terminal of the FET is connected to the output port (see claim 4, lines 3-5), and as discussed above, Fig. 1 of Sudo does not show this claim limitation. Furthermore, claim 4 recites the operation of the FET in it sub-threshold region when in steady state and when the input signal voltage is stationary. As discussed with respect to claim 2, this is not taught or suggested by Sudo.

Accordingly, claim 4 is believed to be patentable over Sudo.

For the same reasons as discussed with respect to claims 2 and 4, claims 8 and 10 are also believed to be patentable over Sudo.

35 U.S.C. §103(a) rejection of claims 3, 5, 6, 9, and 11 over Sudo

These claims contain the limitation that the FET has a leakage current in excess of 1 micro ampere per micron of device width. As discussed above, the present invention is believed novel because it makes use of leakage current to perform maximum or minimum detection. This is somewhat counter-intuitive, because leakage current is usually considered a problem for most circuits. The circuit of Sudo is not relevant to claims 3, 5, 6, 9, and 11. As discussed above, Sudo teaches a voltage booster, and one of ordinary skill in the art would infer that the devices taught in Sudo operate in their active regions. There simply is no motivation, upon reading Sudo, to practice the claimed invention for which the FET has a leakage current in excess of 1 micro ampere per micron of device width.

Accordingly, claims 3, 5, 6, 9, and 11 are believed patentable over Sudo.

35 U.S.C. §103(a) rejection of claims 6 and 12 over the admitted prior art (Figs. 1-4) in view of Nakano

Nakano is cited in the Office Action for teaching field effect transistors that are substituted for diodes. (See the Office Action, top of page 5.) However, nowhere does Nakano teach or suggest a FET having a leakage current in excess of 1 micro ampere per

micron of device width. As discussed above, Sudo is not applicable to the presently active claims, and therefore, the combination of Nakano and Sudo do not teach or suggest claims 6 and 12.

Applicants believe that all presently active claims are patentable over the cited references.

Respectfully submitted,

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Version of Amended Claims Showing Changes

2. (Amended) [The] A circuit comprising: [as set forth in claim 1,]

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port so that the output voltage is indicative of a local time-average maximum of the input signal voltage; and

wherein in steady state the FET is coupled to operate in a sub-threshold region if the input signal voltage is stationary.

3. (Amended) [The] A circuit comprising: [as set forth in claim 1,]

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port so that the output voltage is indicative of a local time-average maximum of the input signal voltage; and

wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

4. (Amended) A method to provide an output voltage indicative of a local time-average maximum of an input signal voltage, the method comprising:

[providing] operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a first terminal, and a second terminal, wherein the gate and the first terminal are each connected to an input port, and the second terminal is connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port.

6. (Amended) A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the gate and the first terminal are each connected to the input port, wherein the second terminal has a DC offset correction voltage, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

8. (Amended) [The] A circuit comprising: [as set forth in claim 7,]

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port so that the output voltage is indicative of a local time-average minimum of the input signal voltage; and

wherein in steady state the FET is coupled to operate in a sub-threshold region if the average voltage is stationary.

9. (Amended) [The] A circuit comprising: [as set forth in claim 7,]

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port; and

wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

10. (Amended) A method to provide an output voltage indicative of a local time-average minimum of an input signal voltage, the method comprising:

[providing] operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a

first terminal, and a second terminal, wherein the first terminal is connected to an input port, and the gate and the second terminal are each connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port.

12. (Amended) A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the first terminal is connected to the input port, wherein the gate and the second terminal are connected to each other and have a DC offset correction voltage; wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

_____ A check in the amount of $_____ is attached for presentation of additional claim(s).

_____ Applicant(s) hereby Petition(s) for an Extension of Time of _____ month(s) pursuant to 37 C.F.R. § 1.136(a).

_X_ A check for $ 130.00 _____ is attached for processing fees under 37 C.F.R. § 1.17(i).

_____ Please charge my Deposit Account No. 02-2666 the amount of $_____.

A duplicate copy of this sheet is enclosed.

_X_ The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 02-2666 **(a duplicate copy of this sheet is enclosed)**:

_X_ Any additional filing fees required under 37 C.F.R. § 1.16 for presentation of extra claims.

_X_ Any extension or petition fees under 37 C.F.R. § 1.17.

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